REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4 and 6-28 remain in the application. Claims 1, 6, 7, and 8 have been amended. Claim 5 has been canceled.

The limitation of claim 5 has been included in independent claim 1.

The dependency of claims 6, 7, and 8 has changed to claim 1.

In item 2 on page 2 of the above-identified Office Action, claims 1-4 and 11-15 have been rejected as being anticipated by Irrinki et al. (U.S. 6,067,262) (hereinafter "Irrinki") under 35 U.S.C. § 102(b).

The rejection has been noted and claim 1, and the dependency of claims 6, 7, and 8 have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in the original claims of the instant application.

As also will be explained below, it is believed that the claims 11-26 were patentable over the cited art in their

previous form and, therefore, those claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method of testing an integrated circuit, by:

providing an integrated circuit that includes a self-test device;

starting to perform a test of the integrated circuit with the self-test device;

taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device; and

subsequently, connecting the integrated circuit to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test.

Irrinki discloses a method for detecting and rejecting faulty integrated circuits using stress factors during the manufacturing production process where the stress factor is applied to an integrated circuit having built in self-test (BIST) circuitry. The BIST is performed on a predetermined portion of the integrated circuit to detect a set of faulty memory locations and those results are stored. A second BIST is performed that generates a second set of faulty memory locations and the second results are stored. The first and second stored results are then compared and if the results differ the integrated circuit is rejected.

Irrinki does not disclose after testing, taking at least parts of the integrated circuit out of operation after the parts have been tested, including not supplying a clock signal or a supply voltage , which is needed to operate or supply the integrated circuit with power, to part of the integrated circuit.

Irrinki does not show "taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device; and subsequently, connecting the integrated circuit to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test" as

recited in claim 1 of the instant application or "a self-test control device for causing testing of the integrated circuit by the self-test device before the integrated circuit is connected to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test" as recited in claim 11 of the instant application.

In item 4 on page 3 of the above-identified Office Action, claims 5-10 have been rejected as being unpatentable over Irrinki in view of Krug (U.S. 4,961,053) under 35 U.S.C. § 103(a).

Claims 6-10 now depend on claim 1 and include the patentably distinguishing feature as discussed above.

In item 6 on page 4 of the above-identified Office Action, claims 16-23 have been rejected as being unpatentable over Krug in view of Irrinki under 35 U.S.C. § 103(a).

In item 7 on page 5 of the above-identified Office Action, claims 24-26 have been rejected as being unpatentable over the admitted prior art in view of Krug and further in view of Irrinki under 35 U.S.C. § 103(a).

The foregoing discussion is equally applicable in the rejections.

The KRUG reference does not show, and in fact specifically teaches against, an integrated circuit including a self-test device as required by independent claims 1, 11, 16, and 24 of the instant. application. In KRUG, col. 2, lines 55 - 57, Fig. 1 is described as "a diagrammatic plan view of a base plate 1 on which a plurality of circuit components 2 to be tested are formed as integrated circuits."

However, in contrast to applicant's present claimed invention, KRUG specifically teaches away from each integrated circuit including its own self-test device. In col. 1, lines 42 - 51 KRUG states:

> Other prior publications have suggested that each circuit component have its own testing circuit permanently built into it. This causes large proportions of area of the circuit components as well as the available external connections of the finished units to be lost. Further, these circuit components have to be tested individually, which is very time consuming. Errors are detected only in the final condition of the circuit component, so that many manufacturing steps required to reach the final condition result in a waste of time.

And, in col. 3, lines 18 - 24, KRUG further states:

> The testing circuit 3 occupies a larger area on the base plate 1 than the individual circuit components 2 **but it saves separate testing circuits which are built into every one of the circuit components** and which together would occupy even a larger area and especially would reduce the number of functional elements of the circuit component. (emphasis added)

The present claimed invention requires not only that each integrated circuit have a self-test circuit built therein, but also that the integrated circuit perform a test before being connected to an external testing device and subsequently making available to an external testing device the results of that test. And independent claims 1 and 16 require taking specific components out of operation after the self testing. KRUG teaches away from using a self-test circuit as part of the individual circuit components. In fact, the teachings of KRUG would be destroyed by constructing integrated circuits having a self-test device or method as recited in the independent claims. KRUG is silent on how the cited prior art devices use the self-test circuit, and further does not teach or suggest the particular elements recited in applicant's claims.

Moreover, there is no basis or justification other than hindsight reconstruction of the prior art relying on applicants invention as to why one skilled in the art would want to combine the features of a reference such as Irrinki,

which discloses self-test circuitry, with a reference like Krug, which does not even show or suggest self-test circuitry.

Further, independent claims 1 and 16, and claims 2-4 and 6-10, and 17-23 depending therefrom, respectively, require, among other limitations, the step of "taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device" and that the integrated circuit include components and "a device for, at a particular time, taking specific ones of said components out of operation". Nowhere does KRUG teach or suggest a system wherein the self-test device is in the integrated circuit itself (specifically taught against in KRUG as discussed above), and having the other elements of applicant's claims. Nor are Irrinki and Krug properly combinable because Krug has nothing to do with self testing of integrated circuitry and there is no motivation or justification in either reference for combining the references as proposed by the Examiner.

Independent claim 24 recites, among other limitations, a wafer comprising a plurality of integrated circuits, each including a self-test device therein. The foregoing discussions of Krug and Irrinki individually and their incompatibility are applicable in the rejection of independent claim 24 and the claims dependent therefrom. Additionally, KRUG is silent on

the particular configuration and/or operation of the prior art devices discussed in that reference. Further, KRUG is silent on the particular details of the electrical interconnections which are required by the instant dependent claims. As such, KRUG neither teaches, nor suggests, the claimed invention of present claim 24, or claims 25 - 28 depending therefrom.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1, 11, 16, or 24. Claims 1, 11, 16, and 24 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1, 11, 16, or 24.

Finally, applicant appreciatively acknowledges the Examiner's statement that claims 27 and 28 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, applicant respectfully believes that rewriting of claims 27 and 28 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-4 and 6-28 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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FDP/bb

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